Silicon wafer thinning, the singulation process, and die strength

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Abstract

In recent years, the realization of the IoT (Internet of Things) society, in which anyone can connect to the network to search for anything at anytime from anywhere, is approaching. For the IoT to progress, semiconductor devices (chips), such as various types of sensors and communication and memory devices, manufactured by forming a circuit on the silicon wafer, are essential. In general, both “thinning” and “minimizing” are required. On the other hand, die strength improvement is also very important for improving the yield of the manufacturing process and enhancing the endurance of the final product. This review explains the die strength of the CMP and DP stress-relief wafer thinning processes and the DBG singulation process.

1. Introduction

During front-end production of semiconductor devices, electronic circuits such as transistors are formed on the surface of a silicon wafer. Subsequently, in back-end production, the wafer backside is thinned and the wafer is singulated by dicing. The chips are then encapsulated in a package that will be delivered to end-users. The need for thinner chips has been growing in recent years to support lower package heights and allow several chips to be stacked and encapsulated in packages.

For wafer thinning, the grinding process with a grinder is normally used from the viewpoints of cost and productivity. Since wafers are ground in the brittle mode, streaks called saw marks as shown in Fig. 1 are created and a damaged layer remains on the processed surface.

In order to remove this damaged layer, a stress relief process, such as chemical mechanical polishing (CMP) and dry polishing (DP), is introduced. CMP uses slurry as an abrasive. DP does not use water or chemicals, including slurry. Consequently, DP excels in terms of cost and environment because it does not require abrasives or recovery and treatment of wastewater.

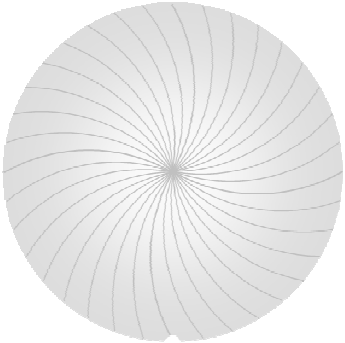

Fig.1 Saw mark image

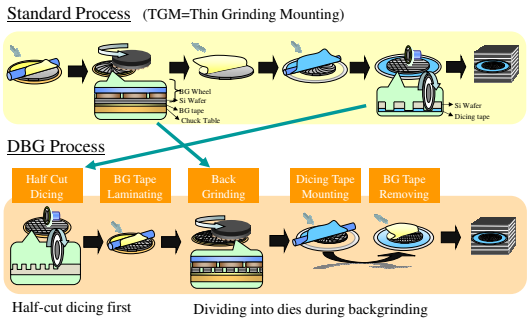

Fig.2 DBG process flow

When a wafer is cut into chips, full-cut dicing with a blade is employed. Since this process also uses the brittle mode, micro-cracks called chippings are generated on the front and rear sides of the wafer. As a countermeasure for this problem, dicing before grinding (DBG) process is also applied. In this process, as shown in Fig. 2, grooving (half-cut dicing) is performed from the front side before grinding. Then, when the half-cut groove is reached during grinding, the wafer is divided into chips.

DBG has an advantage in that backside chipping can be greatly reduced since the damaged layer on the backside caused by the half-cut dicing is eliminated by the grinding process. Fig. 3 shows the difference between the backside chipping for standard and DBG processes.

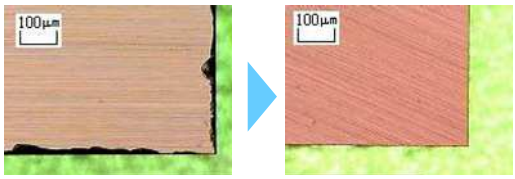

Fig.3 Photos showing backside chipping comparison

Through these processes, memory chips used in smartphones and tablets can now be thinned to below 100 μm. However, wafers and chips are sometimes broken in the manufacturing process, which deteriorates the yield. Therefore, improvement in the die (chip) strength is required at the same time. This review will explain the die strength at each stage of the semiconductor production process.

2. Evaluation method

As a method of measuring the die strength, Semiconductor Equipment and Materials International (SEMI) has specified the standard of 3-point bending as G86-0303[1]. In the 3-point bending test, as shown in Fig. 4, a chip is simply supported without securing both ends and a vertical load is continuously applied with an indenter until the chip is broken. When the chip breaks, the load is recorded as the maximum load. On the upper side of the chip, compressive stress is applied while tensile stress is generated on the lower side. Generally, brittle materials have higher compressive stress than tensile stress. Thus, this test observes the tensile stress on the lower side. The maximum breaking load is calculated as a bending stress value per unit area with Equation 1.

$$\sigma_{fb} = \frac{3P_B L}{2bh^2} \quad \text{(Equation 1)}$$

Although SEMI has also defined G96-1014[2] as the standard of cantilever bending test, the more commonly used 3-point bending test was employed in this review.

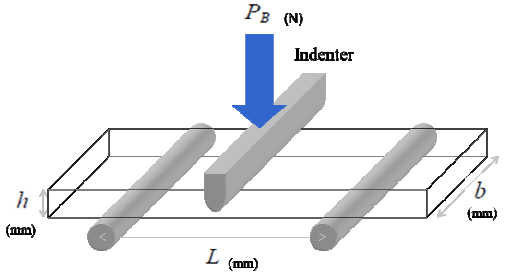

Fig.4 Die strength measurement by 3-point bending

3. Evaluation results

3.1 Influence of saw marks

As mentioned above, due to grinding during wafer thinning, saw marks remain. Since they are formed radially from the center, each chip has a different saw mark angle. Because of this, the influence of saw mark angles on the 3-point bending die strength test was evaluated. Die strength was measured for 20 chips each at three saw mark angles: 0º, which is parallel to the indenter of the 3-point bending test, 45º, and 90º, which crosses the indenter at right angle. For grinding, wafers were thinned to 200 μm using the #2000 and #4800 grinding wheels. For dicing, the standard full cut was performed.

As shown in Fig. 5, chip strength decreased dramatically at 0º (when the indenter is parallel to the saw mark). When comparing chips processed with the #2000 wheel between 0º and 90º, the minimum value of the latter is 2.3 times higher than the former. This result clearly shows that the die strength is influenced by the saw mark angles.

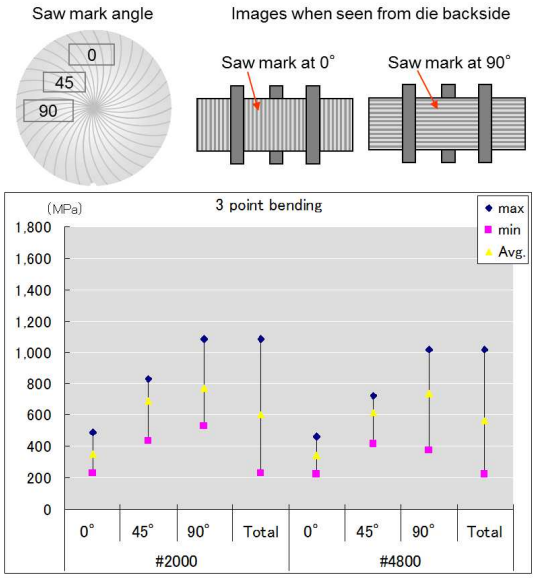

Fig.5 Die strength by 3-point bending (saw mark angle comparison)

3.2 Effect of stress relief

Next, the effect of stress relief for removing grinding damage and saw marks to have a mirror surface was evaluated. A layer of approximately 2 μm was removed using the abovementioned CMP and DP to have a mirror surface after grinding

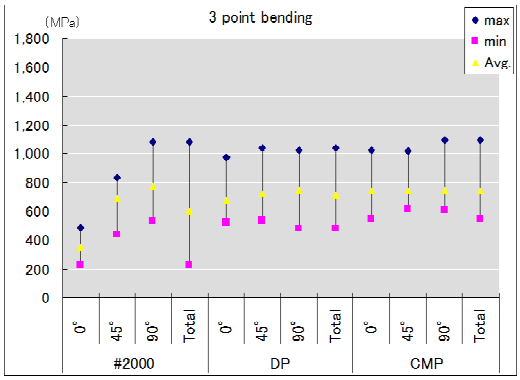

Fig.6 Die strength by 3-point bending (stress relief comparison)

with the #2000 wheel. For dicing, the standard full cut was used again.

As a result, die strength independent of saw marks could be obtained (Fig. 6). No difference in the die strength between CMP and DP could be found. However, although grinding damage was removed, the average and maximum values of strength were not substantially improved. This point suggests that factors other than the chip backside condition may influence the results of the 3-point bending test.

3.3 Influence of backside chipping

Lastly, the influence of chipping generated on the four sides of chip backside was evaluated. Comparative samples were made using the DBG process, which can greatly reduce backside chipping. For the backside condition of chips, the surfaces processed with the #2000 and DP wheels were evaluated.

As shown in Fig. 7, there was no difference between standard full cut dicing and DBG for the backside condition of chips processed with the #2000 wheel. However, on the DP processed surface, die strength was increased due to the greatly reduced backside chipping by DBG.

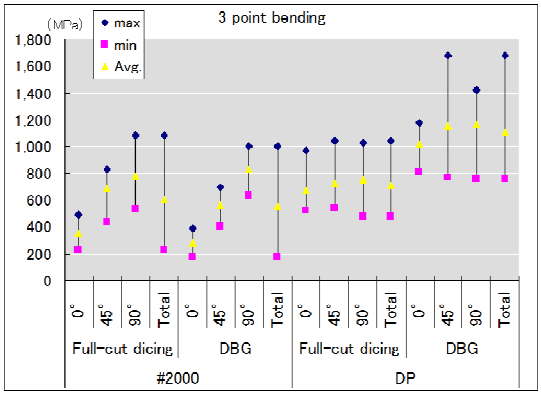

Fig.7 Die strength by 3-point bending (backside chipping comparison)

3.4 Summary

The 3-point bending test results reveal that improving grinding damage (saw mark angle) on the chip backside, first of all, enables increasing the minimum values of chip strength. By reducing the backside chipping after that, the overall strength could be enhanced. The best results could be obtained by the DBG + DP process.

4. Conclusion

The need for thinning of semiconductor chips is becoming more intense. A size of 30 µm or less is required in some cases and therefore higher die (chip) strength becomes more important. Naturally, damage sustained in chips must be reduced using the lowest cost possible. Identifying the proprieties of factors influencing the chip strength is therefore very important. We will further evaluate influencing factors at the sides and front surface of the chips.

References

[1] SEMI G86-0303 : 2011. TEST METHOD FOR MEASUREMENT OF CHIP (DIE) STRENGTH BY MEAN OF 3-POINT BENDING
[2] SEMI G96-1014 : 2014. TEST METHOD FOR MEASUREMENT OF CHIP (DIE) STRENGTH BY MEAN OF CANTILEVER BENDIN

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